Simulation-aided Analysis

of Reliablity Risks and Failure Mechanisms

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Agenda

- Analysis approaches and prerequisites
- Circuit specific investigations
- Simulation-aided approach
- Analysis examples
- Process flow
- Summary

Assumption

- **Implicit assumption of fault analysis**
  - Devices and circuitry are working under adapted operating conditions
  - Devices and circuitry are running inside specification

⇒ **Fault conditions are caused by irregular, exeptional events (?)**

Single Point of Failure

- **Assumption is correct in case of**
  - EOS – improper handling of electronic modules, faulty elements are causing overstress or operation outside device specification
  - ESD – short-time high-voltage discharges are causing stress outside operating conditions

Circuit Specific Stress

- **Existing applications can contain**
  - short time out-of-spec conditions
  - spikes
  - voltage or current peaks

- **Device conditions are causing**
  - degeneration
  - early wear out
  - life time shortening
  - destruction by over-stress

Circuit Investigation and Extract

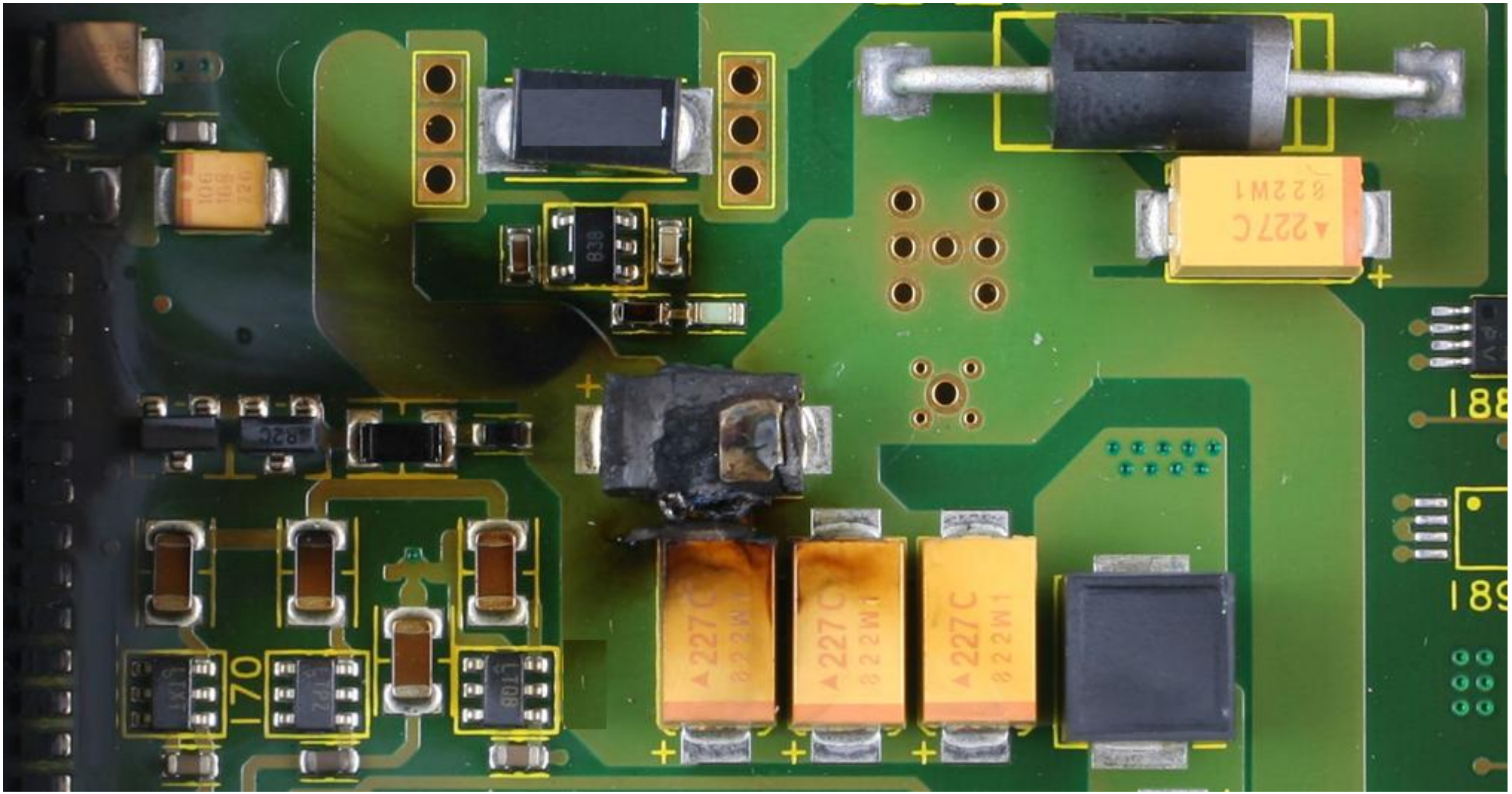
- **Close environment of failing devices**
  - Regard during analysis
  - Environmental analysis already during fault localization

- **Modeling of affected part of circuit**
  - Circuit extract as simple as possible to reduce overhead
  - Simulation case only for suspected fault case

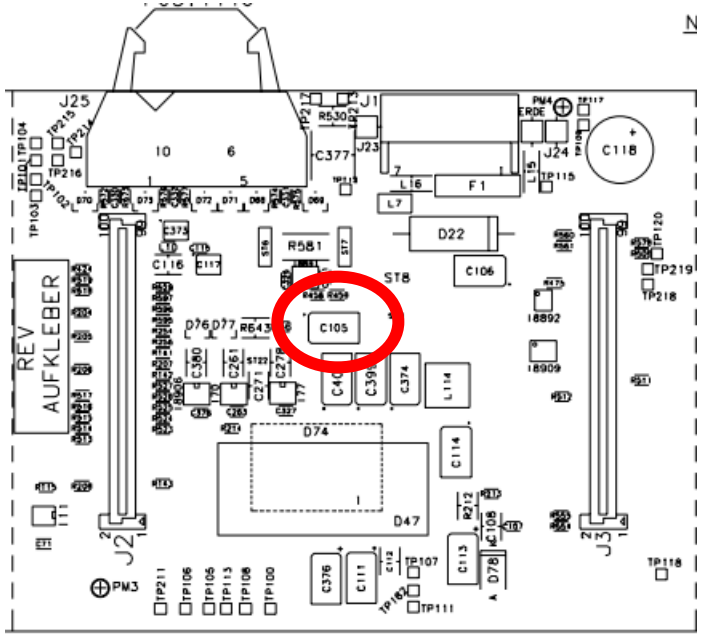
Methodology of Circuit Analysis

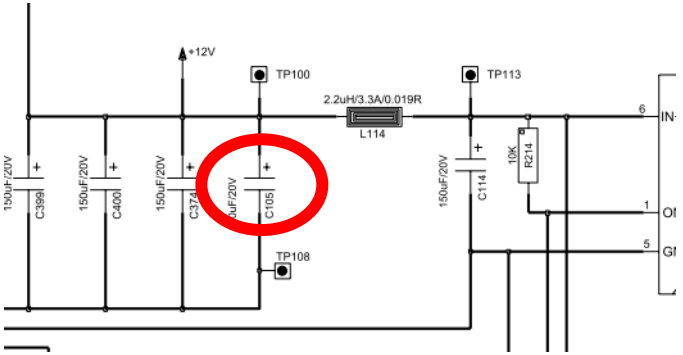
- **Circuit specific investigation**
  - Evaluation of fault case
  - Collection of potential root causes
  - Assessment of part of circuitry in which the fail occurs
  - Evaluation of parametric and functional wiring
  - Calculation and simulation

Device Destruction

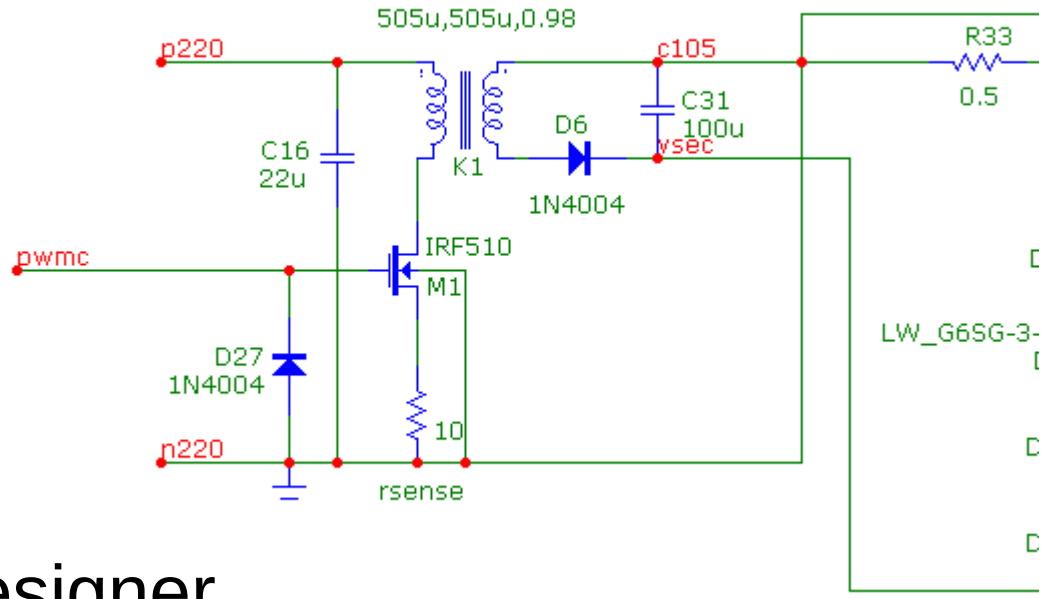


Destructed Part and Close Environment





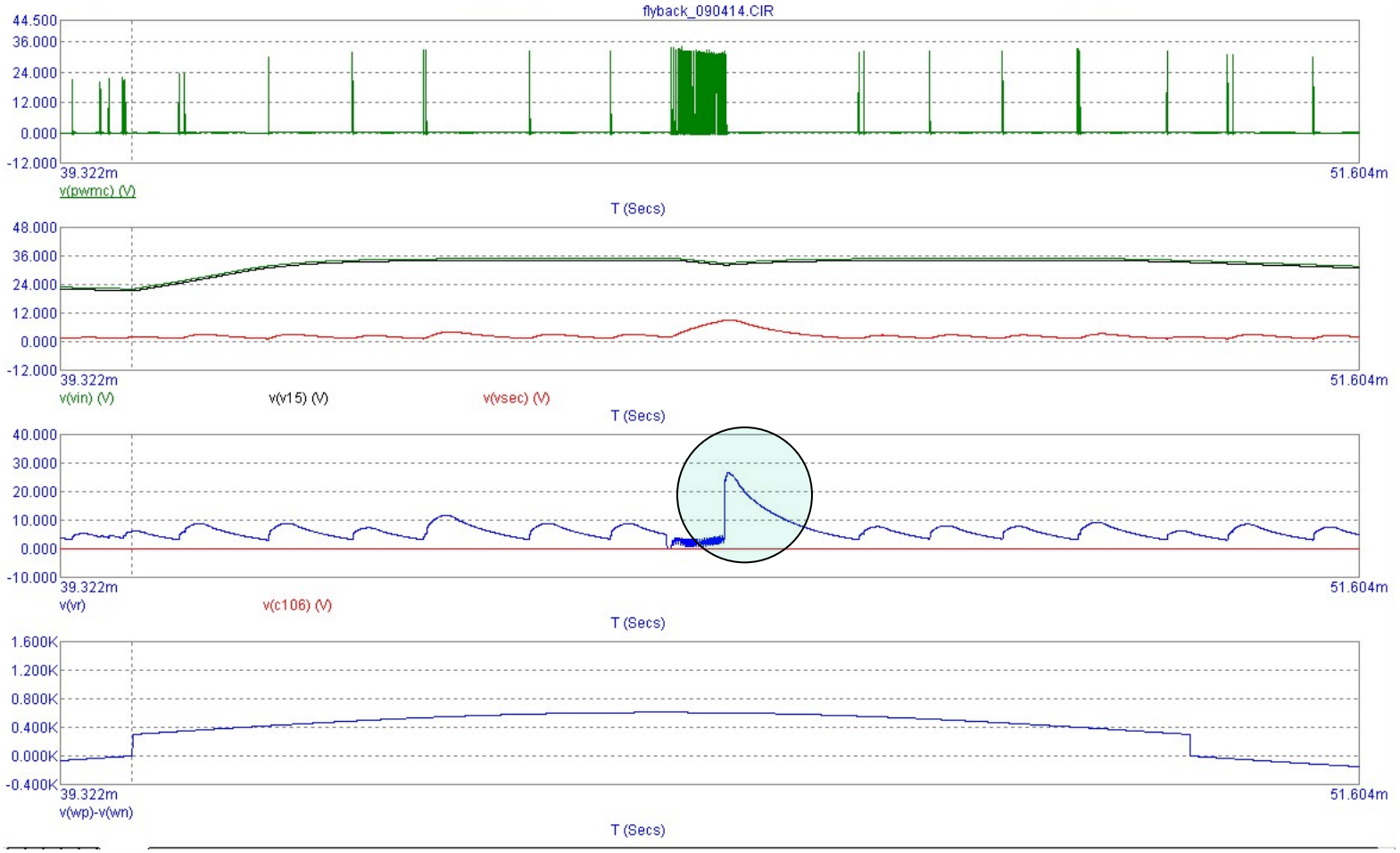
Modeling



Tools:

- Altium Designer
- Spektrum Micro-Cap
- PSpice

Simulation Voltage Peak at Capacitor



Specification Cross-Check

RATINGS & PART NUMBER REFERENCE

AVX Part No.	Case Size	Capacitance (µF)	Rated Voltage (V)	DCL (µA) Max.	DF % Max.	ESR Max. (mΩ) @100kHz	100kHz Ripple Current R	
							25°C	85°C
TPSB107*002#0200	B	100	2.5	5	6	200	0.652	0.587
TPSB157*002#0150	B	150	2.5	3	10	150	0.753	0.677
TPSB227*002#0150	B	220	2.5	4.4	16	150	0.753	0.677
TPSB227*002#0200	B	220	2.5	4.4	16	200	0.652	0.587
TPSB227*002#0600	B	220	2.5	4.4	16	600	0.376	0.339
TPSD227*002#0045	D	220	2.5	4.4	8	45	1.826	1.643
TPSY337*002#0040	Y	330	2.5	8.2	8	40	1.768	1.591
TPSD477*002#0035	D	470	2.5	11.6	8	35	2.070	1.863

Cap. (µF)	Rated volt. 16 VDC						
	Part No.	Dimensions (mm)			Size Code	Q'ty
		L	W	H		
0.00010	ECHU1C101□X5	1.6	0.8	0.7	K1	
0.00012	ECHU1C121□X5	1.6	0.8	0.7	K1	
0.00015	ECHU1C151□X5	1.6	0.8	0.7	K1	
0.00018	ECHU1C181□X5	1.6	0.8	0.7	K1	
0.00022	ECHU1C221□X5	1.6	0.8	0.7	K1	
0.00027	ECHU1C271□X5	1.6	0.8	0.7	K1	
0.00033	ECHU1C331□X5	1.6	0.8	0.7	K1	

Verification Path

Non-Destructive Analysis

- Electrical Analysis
- Parametrical Analysis
- Fault localization
- X-Ray

Modelling

- Circuit extration
- Simplification
- Simulation

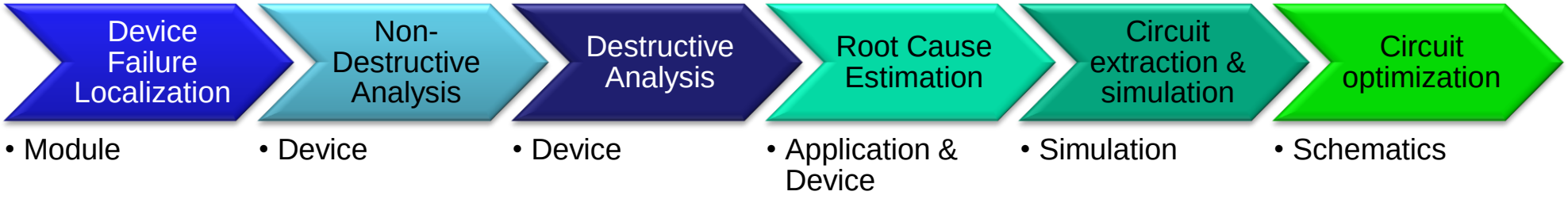
Destructive Analysis

- SAM
- SEM
- FIB
- OBIRCH

Circuit Optimization

- Parametric adaptation
- Bias point shift
- Protection circuitry

Process Flow Circuit Optimization



Final Assessment

- **Results of analysis can be used for**
  - circuit optimization
  - parametric changes
  - bias point adaptation
  - peak attenuation
  - spike prevention
  - implementation of protective circuitries

Summary

- **Structural analysis needs to**
  - Put wiring of failing device in focus
- **Modelling and simulation can**
  - Help to better understand fault case
  - Reproduce failure condition
- **Learning from analysis can**
  - Be used for improvements of failing module
  - Be used for optimization and debugging

Thanks a lot for your attention & patience!

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